

expressXG Framework Lite for High-Bandwidth FPGA Applications

Benefits

- Mitigates the complexity and scheduling risks associated with implementing high bandwidth applications
- Enables developers to focus on implementing their applications rather than learning details of lower level, Ethernet and physical interface implementation
- Ensures effortless migration across platforms, while preserving in-house development efforts
- Safeguards capital investment in network monitoring and security infrastructure

Features

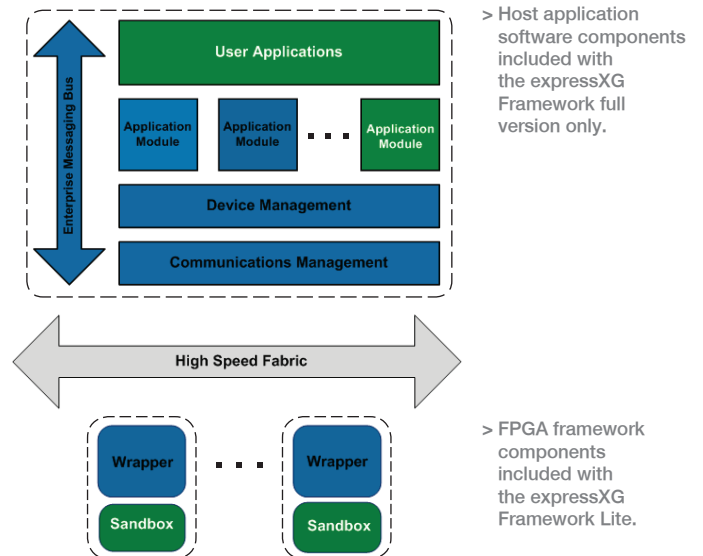
- Synthesized wrapper providing simple and robust user interface to high-performance communication controllers
- Sandbox sample applications and debug capabilities to develop FPGA applications “out of the box”
- 10 Gigabit Ethernet controller featuring advanced Layer 3 and Layer 4 protocol processing
- DDR2 SDRAM and SRAM communication controllers
- PCI Express® endpoint controller supporting x4 or x8 configurations
- Low-latency peripheral controller for host control over 1 Gigabit Ethernet
- In-system programming with remote configuration capabilities

Applications

- Network Security
- Network Monitoring
- Sensor Systems

Overview

The expressXG™ Framework Lite is an FPGA development framework that enables customers to rapidly create and deploy high-bandwidth applications on a broad range of AdvancedIO’s platforms. With advancements in silicon technology, FPGAs today offer an unmatched capability for providing optimized solutions to the challenging problems encountered in high-bandwidth, real-time packet and signal processing applications, such as network monitoring and situational awareness. However, programming FPGAs typically requires more effort and a specialized skill-set than that required to create software for single or multi-core processors. In addition, significant effort investment is required to learn the documented and undocumented nuances of implementing viable Ethernet communications using FPGAs, especially at very high speeds. These characteristics may increase FPGAs’ perceived risk and implementation timeframes, causing some project managers and teams to avoid using them and instead settle for sub-optimal software implementations.



> Modular in design, the expressXG Framework Lite is scalable and seamlessly compatible with AdvancedIO's expressXG Framework, which provides rich host application software and DPI capabilities.

Please contact us for software upgrade information.

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Choosing expressXG Framework Lite not only alleviates these concerns, but also provides an exceptional performance-to-cost ratio for high-bandwidth FPGA applications saving thousands of dollars in third-party IP cores integration and licensing fees.

Conceptually, the expressXG Framework Lite consists of an interface wrapper and user sandbox. The wrapper provides a simple and robust user interface to various high-performance controllers, such as the 10 Gigabit Ethernet controller and SDRAM controller. The sandbox is a structural guideline, with sample applications and debugging capabilities, that significantly simplifies and accelerates application coding and integration.

Quickly Integrate DPI Algorithms onto FPGAs

AdvancedIO’s expressXG Framework Lite is ideally suited for government customers who want to rapidly implement their own DPI algorithms onto FPGAs while mitigating many of the associated risks. The framework abstracts underlying hardware interfaces and 10 Gigabit Ethernet communications protocol functions, so developers can focus 100-percent of their time on application development and integration. Using the expressXG Framework Lite environment ensures application portability among FPGA device families on AdvancedIO’s platforms, which reduces the costs of future migration or upgrade cycles significantly. Importantly, all in-house development efforts are preserved and kept confidential.

Upgrade from expressXG Framework Lite to Full Version

The expressXG Framework provides an array of system management configuration, and programming capabilities designed to meet the needs of today’s complex high-bandwidth network situational awareness applications. The framework’s

innovative architecture integrated with AdvancedIO’s deep packet inspection line-speed technology provides a groundbreaking combination of application simplicity, performance and scalability across platforms.

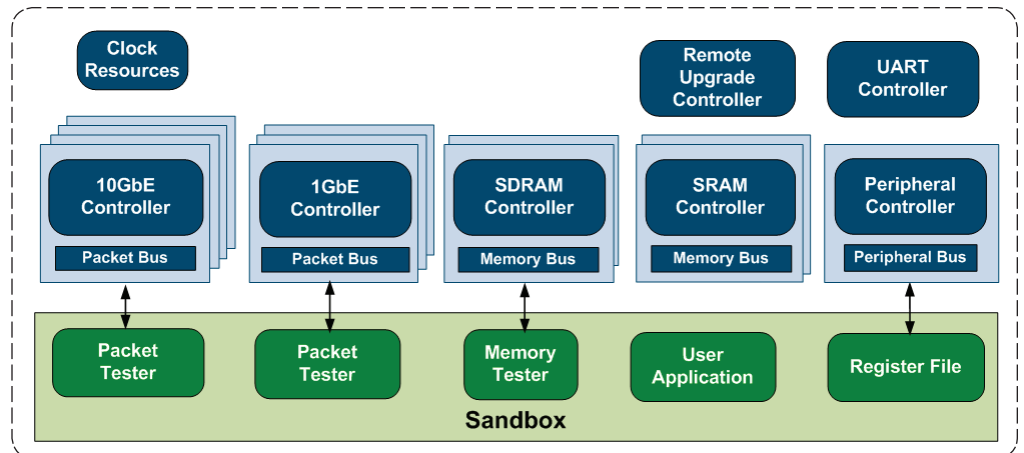
The lite version provides the necessary infrastructure to quickly begin developing DPI functionality on FPGAs. Customers may upgrade to the full version to benefit from its rich software capabilities, such as device drivers, high level APIs, and communication protocol-specific application modules, or may choose to create their own compatible host software.

Versatile FPGA Framework

The framework’s interface wrapper is delivered as a synthesized netlist for any given AdvancedIO platform. Although the wrapper may include a variety of high-performance interfaces, only those available on the platform are used and the remaining interfaces are optimized out (without breaking the framework’s functionality) during user design synthesis. Depending on the platform, one or more of the following interfaces and controllers are included in expressXG Framework Lite:

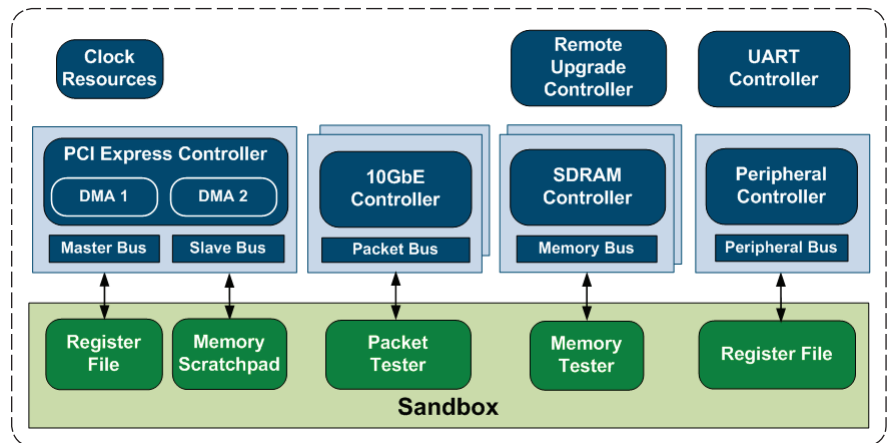
- **10 Gigabit Controller** — is a single-channel, high-performance 10 Gigabit Ethernet controller supporting IEEE 802.3ae implementations and jumbo frames up to 9600 bytes. It has an integrated Gigabit Ethernet Media Access Control (MAC) and XAUI port, making it ideal for chip-to-chip and chip-to-optical module applications. The controller supports external PHY devices for emerging SFP+ line-card applications. In addition to managing the PHY and MAC functions, the controller supports an advanced feature-set that enables it to perform real-time Layer 3 and Layer 4 protocol parsing to extract specific headers for various types of protocols, such as IPv4, TCP, and UDP.

> This detailed view of the FPGA device for XAUI configuration, shows the expressXG Framework Lite’s architecture on the V3021 platform. Top row components (in blue) are provided by AdvancedIO as part of the Framework. Bottom row components (in green) are provided as an infrastructure for developers to begin programming FPGAs.



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> This detailed view of the FPGA device for PCI Express configuration, shows the expressXG Framework Lite's architecture on the V1121 platform. Top row components (in blue) are provided by AdvancedIO as part of the Framework. Bottom row components (in green) are provided as an infrastructure for developers to begin programming FPGAs.



The controller also has a built-in UDP protocol offload engine (UOE) that performs all of the functions required for transmission and reception of UDP packets. The UOE supports up to 32 sockets, each of which can be configured individually to communicate with a unique pre-specified destination. Please contact us for more details.

- **SDRAM Controller** — is a high-performance, low latency memory controller that interfaces with industry standard DDR2 SDRAM memories. It performs all initialization, refresh and power-down functions. The memory controller provides a simple interface that reduces the effort to integrate applications with SDRAM memory. Typically, the memory architecture is 64 bits wide but may vary depending on the platform. The user interface of the controller is 256 bits wide and runs at 133MHz supporting a maximum aggregate bandwidth of 4GB/s.
- **SRAM Controller** — is a high-performance, low latency memory controller that interfaces with industry standard DDR2 SRAM memories. It is capable of automatically managing single address and continuous burst to DDR2 SRAM memory. The controller provides a simple interface that reduces the effort to integrate applications with SRAM memory. The interface is 18 bits wide and runs at 233MHz supporting a maximum aggregate bandwidth of 8.3Gb/s.
- **PCI Express Controller** — is a high-performance PCI Express v2.0 (2.5 GT/s) endpoint controller, supporting x8 and x4 configurations at a speed of 2.5 GHz. The maximum aggregated raw bandwidth for typical x8 configuration is 16 Gb/s in each direction. The controller supports 64-bit addressing and has DMA-master capabilities. This controller is only available for applications requiring PCI Express communication.

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- 1 Gigabit Controller** — is a single-channel Gigabit Ethernet supporting 10/100/1000Base-T and 1000Base-BX implementations. The controller supports external PHY devices capable 10/100/1000Base-T Ethernet on CAT 5 twisted pair cable. It has an integrated Gigabit Ethernet Media Access Control (MAC). In addition to managing the PHY and MAC functions, the controller supports an advanced feature-set that enables it to perform real-time Layer 3 and Layer 4 protocol parsing to extract specific headers for varying types of protocols, such as IPv4, TCP, and UDP. Please contact us for more details.
- Peripheral Bus** — is a 32-bit multiplexed bus that provides read/write access to registers of various controllers in the system, such as the 10 Gigabit controller. For maximum flexibility, registers can be accessed over the Peripheral Bus from the PCI Express, 1 Gigabit Ethernet, RS232 interfaces, or an application running in the sandbox.
- UART Controller** — supports RS232 serial communication, and is primarily used for debugging purposes.

RESOURCE UTILIZATION

	expressXG Framework Lite			Xilinx XC5VLX110T		
	FFs	LUTs	BRAMs	FFs (%)	LUTs (%)	BRAMs (%)
10GbE Controller	1776	1303	0	2.6	1.9	0
2x 1GbE Controller	8246	6177	1	11.9	8.9	0.3
SDRAM Controller	10102	6252	32	14.6	9.0	10.8
SRAM Controller	926	583	7	1.3	0.8	2.4
PCI Express Controller	7604	6634	88	11.0	9.6	29.7
Peripheral Controller	77	63	0	0.1	0.1	0
Total	28731	21012	128	41.5	30.3	43.2

Note: Resource utilization is provided for general design guidance. Actual utilization may vary slightly, depending on functionality.

Technical Specifications

SUPPORTED FPGA DEVICES

The expressXG Framework Lite is compatible with AdvancedIO's platforms supporting a broad range of high-performance FPGA devices from vendors such as Xilinx and Altera. Please contact us for more details.

DESIGN FILE FORMAT

NGC netlist

CONSTRAINTS FILE

UCF

DESIGN TOOLS

Xilinx ISE, Synplicity, ModelSim

ORDERING INFORMATION

expressXG Framework Lite requires an AdvancedIO platform. Software support requires upgrade to full version of expressXG Framework.

FOR MORE INFORMATION ON OUR PRODUCTS:

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